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Dated: October 27, 2003

Docket No.: SCEI 3.0-004 CONT  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:  
Oka et al.

Application No.: Not Yet Assigned

Group Art Unit: N/A

Filed: Herewith

Examiner: Not Yet Assigned

For: GAME SYSTEM WITH GRAPHICS  
PROCESSOR

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**


Dear Sir:

It is respectfully requested that the references listed on the enclosed form be made of record and considered with respect to the above-referenced U.S. patent application. A copy of each reference is of record in Application No. 09/502,671, filed February 11, 2000, the benefit of which is claimed under §120. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited references are legally available prior art or that the same are pertinent or material.

In the event that any fee is due in connection with the present Information Disclosure Statement, the Commissioner is hereby authorized to charge the same to our Deposit Account No. 12-1095.

Dated: October 27, 2003

Respectfully submitted,

By   
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Substitute for form 1449A/B/PTO  <b>INFORMATION DISCLOSURE  STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				<b>C mplete if Kn wn</b>	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Masaaki Oka
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	2	Attorney Docket Number	SCEI 3.0-004 CONT

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	AA**	US-5,319,606	06/1994	Bowen et al.	
	AB**	US-5,900,887	05/1999	Leung et al.	
	AC**	US-6,366,272	04/2002	Rosenberg et al.	
	AD**	US-6,570,571	05/2003	Morozumi, Yuichi	
	AE**	US-5,724,560	03/1998	Johns et al.	
	AF**	US-6,259,431	07/2001	Futatsugi et al.	
	AG**	US-5,977,997	11/1999	Vainsencher, Leonardo	
	AH**	US-6,485,369	11/2002	Kondo et al.	
	AI**	US-5,136,664	08/1992	Bersack et al.	
	AJ**	US-6,384,833	05/2002	Denneau et al.	
	AK**	US-5,467,459	11/1995	Alexander et al.	
	AL**	US-5,995,111	11/1999	Morioka et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)				
	BA**	CA-1,304,509		Baldwin		
	BB**	CA-1,198,523		Neches et al.		
	BC**	CA-2,178,454		Horst		
	BD**	JP-9035084	02-07-1997			
	BE**	JP-10003466	01-06-1998			
	BF**	EP-0 867809	09-30-1998			
	BG**	EP-0 871142	10-14-1998			
	BH**	EP-0 715279-A2	06-05-1996			
	BI**	EP-0 715277-A2	06-05-1996			

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Examiner Signature		Date Considered	
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				Art Unit	N/A
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Sheet	2	of	2	Attorney Docket Number	SCEI 3.0-004 CONT

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>2</sup>
	CA**	KEN KUTARAGI, et al., "A Microprocessor with a 128b CPU, 10 Floating-Point MACs, 4 Floating-Point Dividers, and an MPEG2 Decoder," 1999 IEEE International Solid-State Circuits Conference, February 15-17, 1999, 1999 Digest of Technical Papers, Volume 42.		
	CB**	KEN KUTARAGI, et al., "A Microprocessor with a 128b CPU, 10 Floating-Point MACs, 4 Floating-Point Dividers, and an MPEG2 Decoder," 1999 IEEE International Solid-State Circuits Conference, February 15-17, 1999, Slide Supplement 1999 to the Digest of Technical Papers, Volume 42.		
	CC**	MASAAKI OKA, et al., "Designing and Programming the Emotion Engine," IEEE Micro, November/December 1999, Volume 19, Number 6, pp. 20-28.		
	CD**	KEITH DIEFENDORFF, "Sony's Emotionally Charged Chip," Microprocessor Report, April 19, 1999, Volume 13, Number 5, pp. 1, 6-11.		
	CE**	MASAKAZU SUZUOKI, et al., "A Microprocessor with a 128-Bit CPU, Ten Floating-Point MAC's, Four Floating-Point Dividers, and an MPEG-2 Decoder," IEEE Journal of Solid-State Circuits, November 1999, Volume 34, Number 11, pp. 1608-1618.		
	CF**	"Sony Computer Entertainment Announces the Development of an I/O Processor for the Next Generation Playstation that Provides 100% Backwards Compatibility," Sony Computer Entertainment Inc. press release, March 2, 1999, Tokyo.		
	CG**	"Sony Computer Entertainment Announces the Design of the Next Generation Playstation System," Sony Computer Entertainment Inc. press release, March 2, 1999, Tokyo.		
	CH**	"Sony Computer Entertainment Announces the Development of the World's Fastest Graphics Rendering Processor Using Embedded Dram Technology," Sony Computer Entertainment Inc. press release, March 2, 1999, Tokyo.		
	CI**	"Sony Computer Entertainment Announces the World's Fastest 128 Bit CPU 'Emotion Engine' for the Next Generation Playstation," Sony Computer Entertainment Inc. press release, March 2, 1999, Tokyo.		

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<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	
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